Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V+**

**4 S16**

**5 S15**

**6 S14**

**7 S13**

**8 S12**

**9 S11**

**10 S10**

**11 S9**

**12 GROUND**

**14 A3**

**15 A2**

**16 A1**

**17 A0**

**18 ENABLE**

**19 S1**

**20 S2**

**21 S3**

**22 S4**

**23 S5**

**24 S6**

**25 S7**

**26 S8**

**27 V-**

**28 DRAIN**

**.077”**

**1 28 27**

**12 14 15 16 17**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**26**

**25**

**24**

**23**

**22**

**21**

**20**

**19**

**18**

**A**

**MASK**

**REF**

**.177”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref: A**

**APPROVED BY: DK DIE SIZE .077” X .177” DATE: 9/23/21**

**MFG: SILICONIX THICKNESS .014” P/N: DG506A**

**DG 10.1.2**

#### Rev B, 7/1